

PROGRAMMABLE WEAK WRITE TEST MODE (PWWTM)
BIAS GENERATION HAVING LOGIC HIGH OUTPUT DEFAULT MODE

ABSTRACT OF THE INVENTION

The present invention employs a bias voltage having a selectable magnitude to
5 bias a weak write pull-down transistor in a write driver of a static random access
memory (SRAM) array. A programmable weak write test mode (PWWTM) bias
generator includes an output signal that is a logic high in a default mode when a
WWTM is not active. When the WWTM is active, the generator output signal is the
bias voltage having the selectable magnitude. The default mode logic high is actively
10 maintained when the generator output is connected to a load, such as the write driver
of the SRAM array. A WWTM-enabled SRAM system includes the PWWTM bias
generator. A method of driving a WWTM-equipped SRAM includes generating and
applying the output signal to a gate of a weak write pull-down transistor of the SRAM
array write driver in the default mode and the WWTM.

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